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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,263	06/26/2003	Benjamin N. Eldridge	P150D1-US	8103
50905	7590	03/01/2006	EXAMINER	
N. KENNETH BURRASTON KIRTON & MCCONKIE P.O. BOX 45120 SALT LAKE CITY, UT 84145-0120			KIM, PAUL D	
			ART UNIT	PAPER NUMBER
			3729	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/609,263	Applicant(s) ELDRIDGE, BENJAMIN N.	
	Examiner Paul D. Kim	Art Unit 3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 December 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 22-57 is/are pending in the application.
- 4a) Of the above claim(s) 41-46 and 48-54 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 22 and 25-39 is/are rejected.
- 7) ☒ Claim(s) 23,24,40, 47 and 55-57 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/26/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is a response to the restriction requirement filed on 12/14/2005.

Response to the Election of Species

1. Applicant's election without traverse of Species B, claims 22-40, 47 and 55-57 in the reply filed on 12/14/2005 is acknowledged.
2. Claims 41-46 and 48-54 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/14/2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 22 and 25-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth (US PAT. 6,238,942) in view of Cobbley et al. (US PAT. 6,329,832).

Farnworth teaches a process of making a multi-chip module comprising steps of: providing a plurality of integrated circuits (12); assembling an electronics module by demountably attaching selected ones of the plurality of integrated circuits to a module substrate (16); testing the demountably assembled module; if the module fails the

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testing: removing at least one of the integrated circuits determined to have caused the failure from the module substrate, replacing the at least one removed integrated circuit with another of the plurality of integrated circuits, and repeating the testing step and, if the module again fails the testing, the removing, replacing, and repeating steps as shown in Fig. 2 (see also col. 1, lines 14-55).

As per claim 25 Farnworth also teaches that each integrated circuit includes a plurality of input/output terminals and a plurality of conductive elongate interconnection elements attached to the input/output terminals, and the module substrate includes a plurality of contact locations (30) for contacting the elongate interconnection elements as shown in Fig. 4.

As per claim 26 Farnworth also teaches a process of bringing elongate interconnection elements attached to the contact integrated circuits into contact with corresponding ones of said contact locations and demountably securing said selected integrated circuits to the module substrate as shown in Fig. 4.

As per claim 27 Farnworth also teaches a process of applying a temporary force (adhesion) to the selected integrated circuits in a general direction of said module substrate.

As per claim 28 Farnworth also teaches a process of removing the temporary force (adhesion) from the selected integrated circuits and moving the at least one integrated circuit (defected IC) away from the module.

As per claim 29 Farnworth also teaches a process of clipping (equivalent with attaching) the selected integrated circuits to the module substrate.

As per claim 30 Farnworth also teaches a process of unclipping (equivalent with detaching) the at least one integrated circuit (defected IC), and moving the at least one integrated circuit away from the module substrate.

As per claim 31 Farnworth also teaches a process of wedging elongate interconnection elements attached to the selected integrated circuits in corresponding ones of the contact locations (wire-bonding) as shown in Fig. 4.

As per claim 32 Farnworth also teaches a process of removing (such as cutting) the elongate interconnection elements attached to the at least one integrated circuit from corresponding ones of the contact locations.

As per claim 33 Farnworth also teaches that the conductive elongate interconnection elements comprise spring contacts (wire bonding) as shown in Fig. 4.

As per claim 34 Farnworth also teaches that the contact locations are contact bond pads as shown in Fig. 4.

As per claim 35 Farnworth also teaches that if the module passes the testing, permanently securing to the module substrate the integrated circuits demountably secured to the module substrate (equivalent with complete and shipping).

As per claim 38 Farnworth also teaches a process of utilizing at least one die edge registration fixture (edge terminal) formed on the module substrate to demountably attach the selected integrated circuits to the module substrate as shown in Fig. 4.

As per claim 39 It should be obvious attaching the elected integrated circuits to the module substrate of Farnworth by utilizing a robotic work cell in order to reduce the error rate to compare with human (see also col. 1, lines 52-55).

However, Farnworth teaches all the limitations as set forth above except testing the assembled module by a selected operating speed. Cobbley et al. teach a process of testing an electronic assembled module by using speed grading of the integrated circuits (col. 3, lines 1-21) for subsequent speed sorting. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify a testing process for the assembled module of Farnworth by using speed grading of the integrated circuits as taught by Cobbley et al. for subsequent speed sorting. Cobbley et al. also teach that an adhesive (epoxy) is applied for permanently securing the integrated circuits to the module substrate (as per claim 37).

Even though either Farnworth or Cobbley et al. fails to teach soldering (as per claim 36) for permanently securing the integrated circuits to the module substrate, At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to apply soldering as recited in the claimed invention because Applicant has not disclosed that soldering as recited in the claimed invention provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with Cobbley et al. because soldering as recited in the claimed invention would perform equally well such as adhesion the integrated circuits to the module substrate in Cobbley et al. Therefore, it would have been an obvious matter of design choice to modify epoxy of Cobbley et al. to obtain the invention as specified in claim 36.

Allowable Subject Matter

5. Claims 23, 24, 40, 47 and 55-57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 22-57 have been considered but are moot in view of the new ground of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul D. Kim whose telephone number is 571-272-4565. The examiner can normally be reached on Monday-Friday between 6:00 AM to 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Paul D Kim
Examiner
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